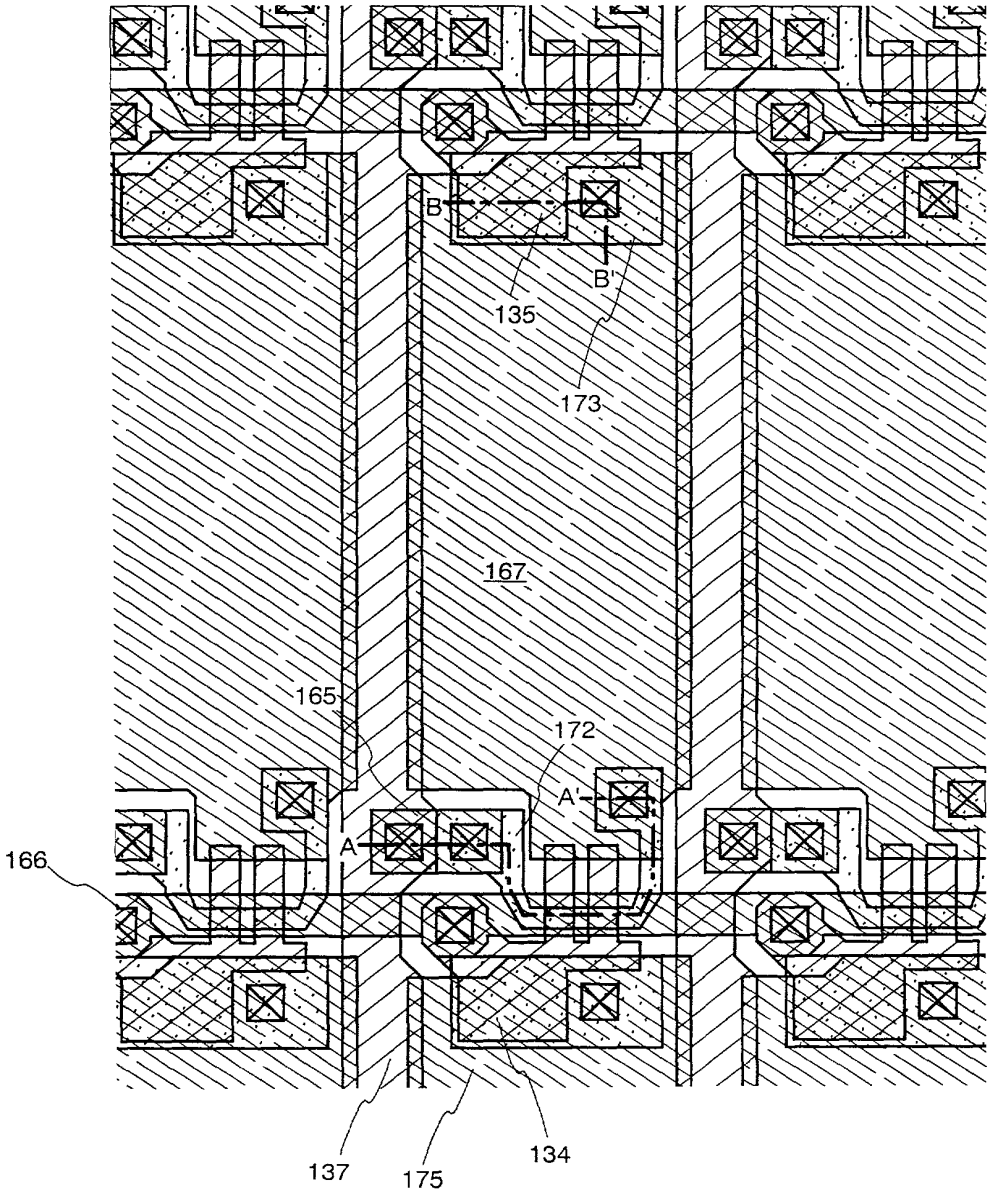


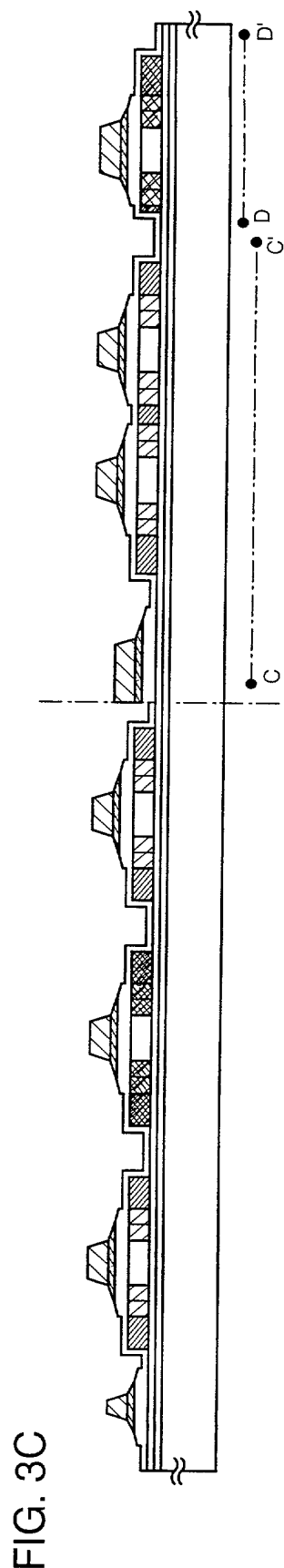
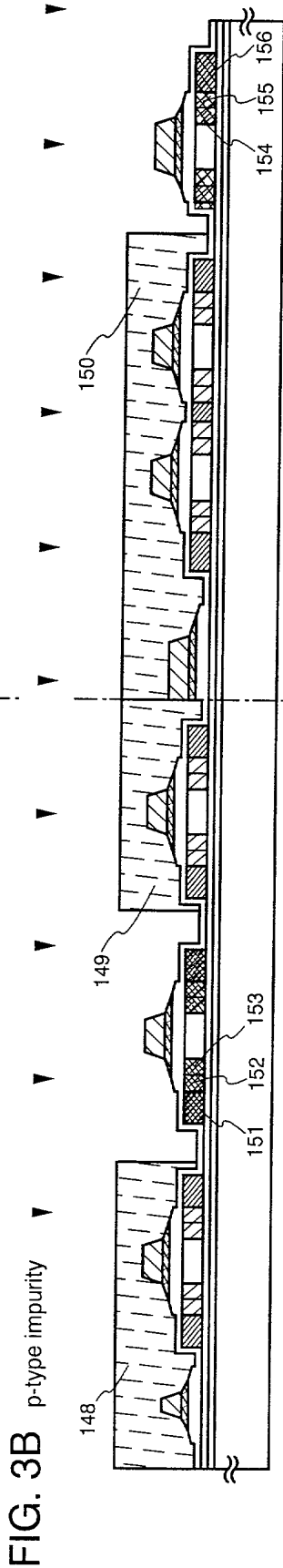
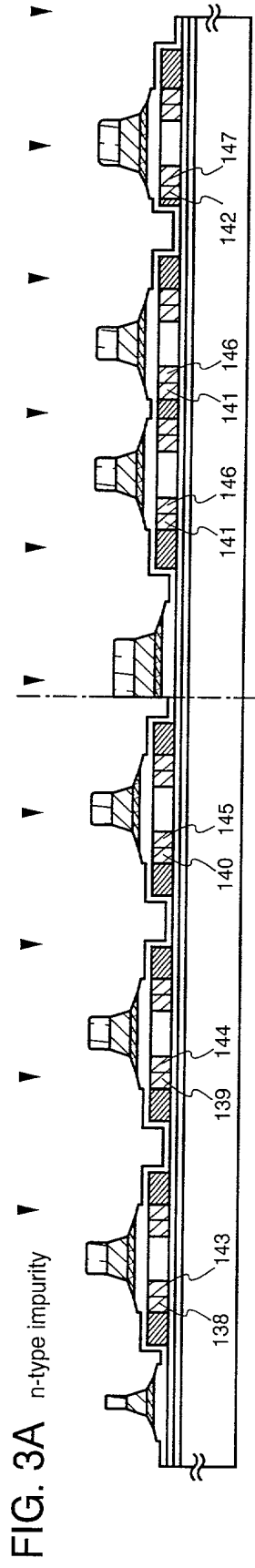
FIG. 1



A cross-sectional view of a multi-layered structure 100. The structure consists of a series of alternating layers: 101a, 101b, 102, 103, 104, 105, and 106. The layers 101a and 101b are grouped together and labeled as 101. The layers 102, 103, 104, 105, and 106 are labeled individually. The interfaces between the layers are labeled 107, 108, and 109. The structure is shown with a top surface 100 and a bottom surface. The layers are separated by interfaces 107, 108, and 109. The layers 101a and 101b are shown with a hatched pattern, while the other layers are shown with a solid pattern. The structure is shown in a perspective view, with a top surface 100 and a bottom surface. The layers are separated by interfaces 107, 108, and 109. The layers 101a and 101b are shown with a hatched pattern, while the other layers are shown with a solid pattern.

2B n-type impurity

Diagram 2B is a cross-sectional view of a semiconductor device. It shows a series of gates and transistors. The gates are labeled 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, and 129. The transistors are labeled 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, and 129. The n-type impurity regions are labeled 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, and 129. The diagram shows a series of gates and transistors with n-type impurity regions.



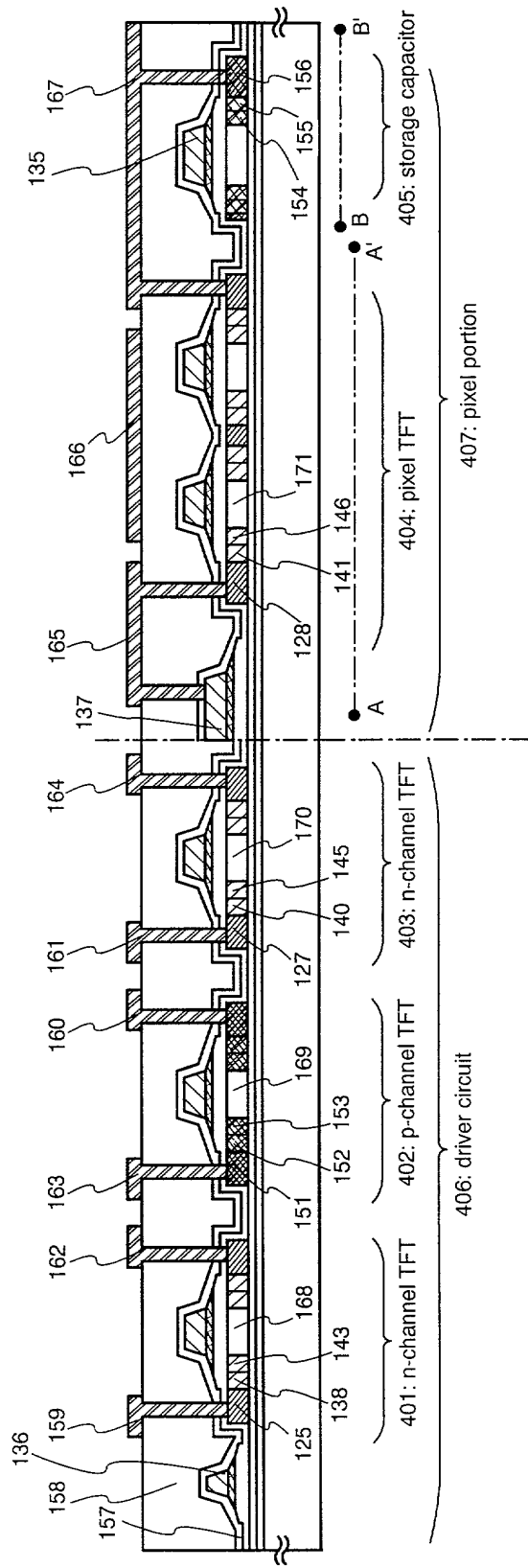


FIG. 4

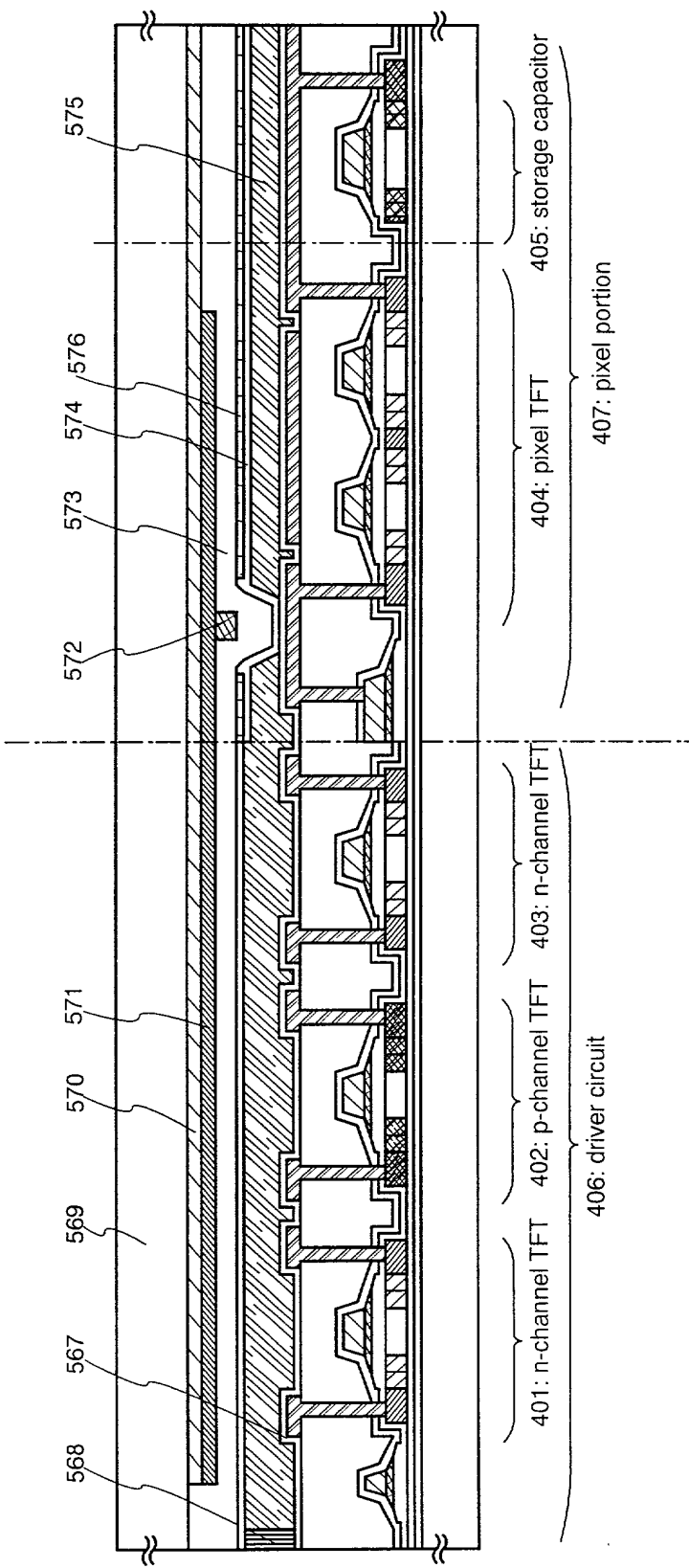
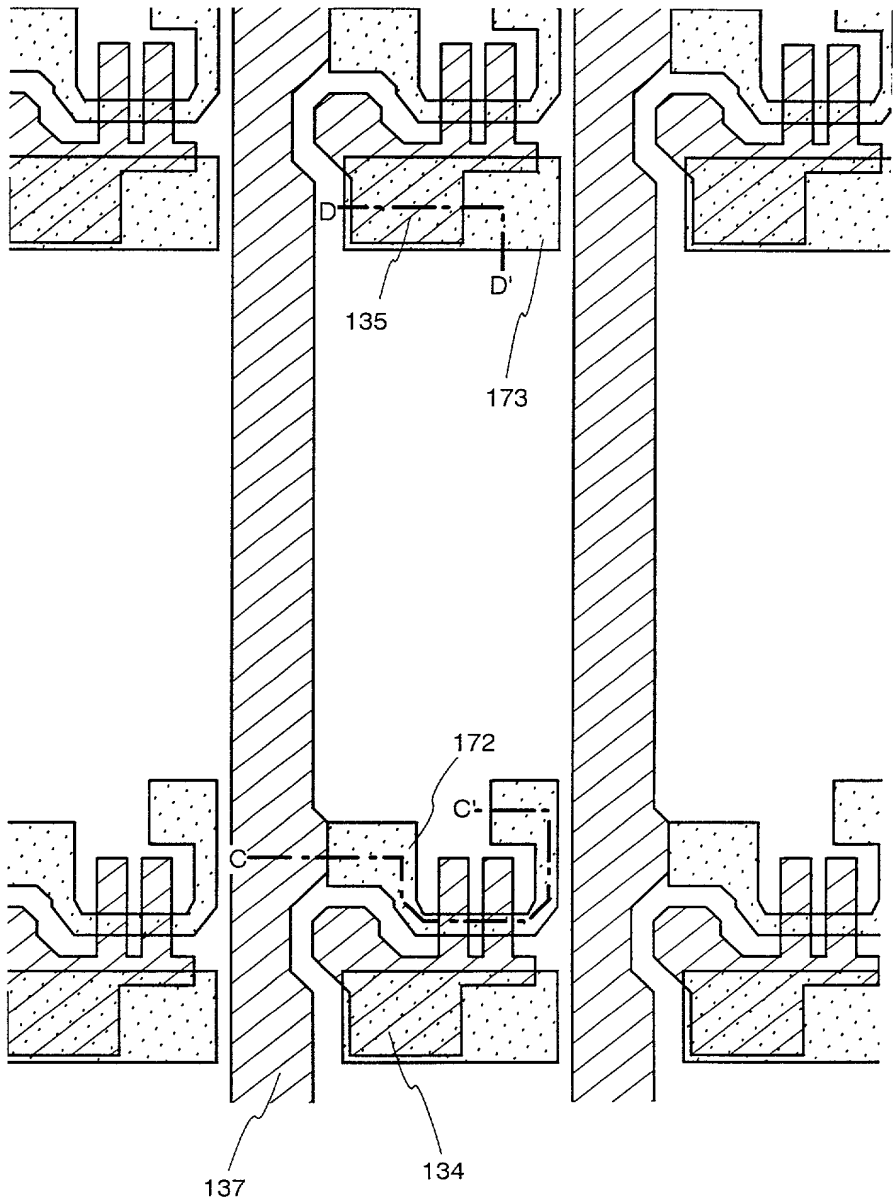


FIG. 5

FIG. 6



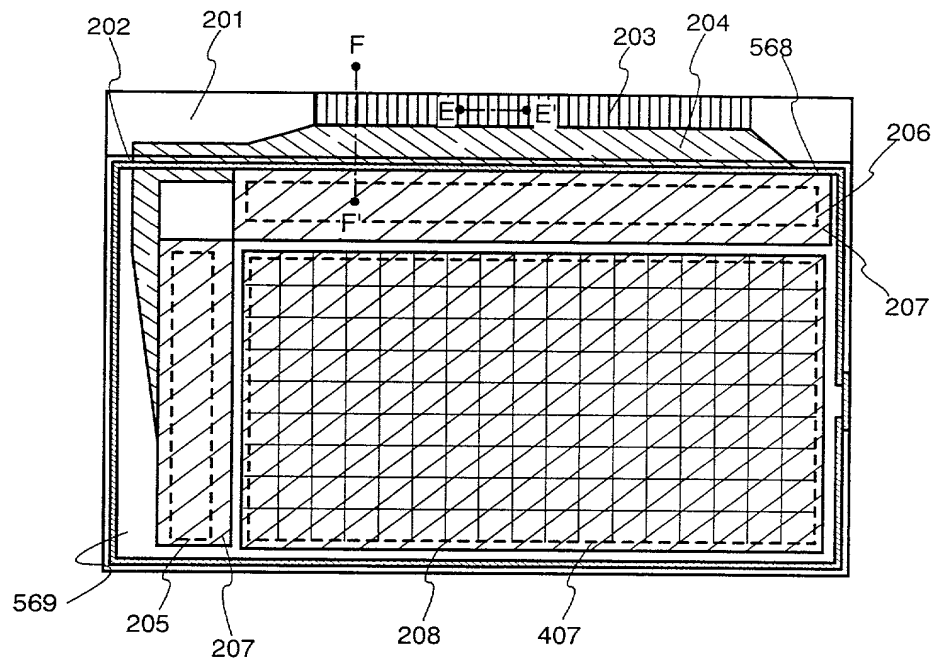


FIG. 7A top view

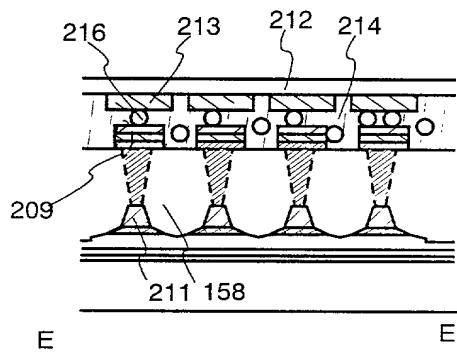


FIG. 7B cross sectional view of E-E'

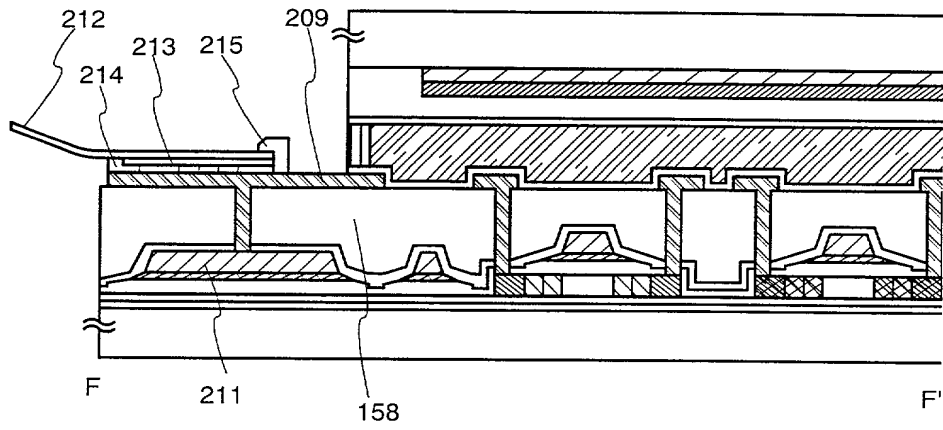


FIG. 8A cross sectional view of F-F'

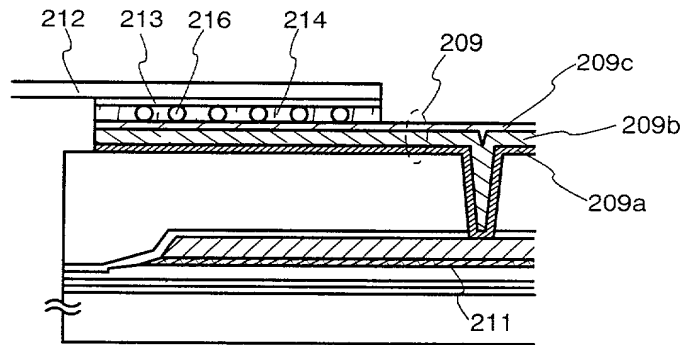


FIG. 8B



FIG. 9A

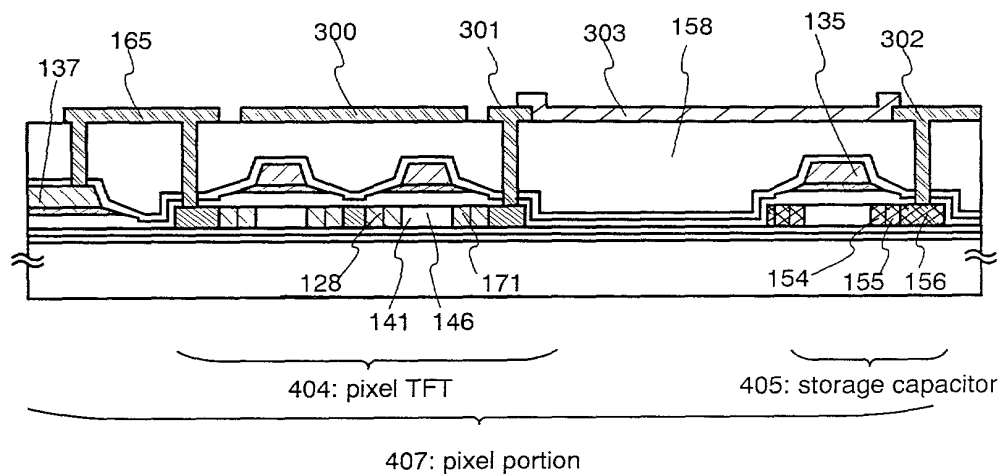


FIG. 9B

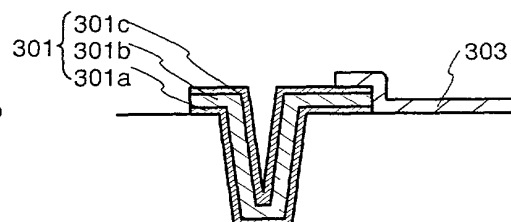


FIG. 9C

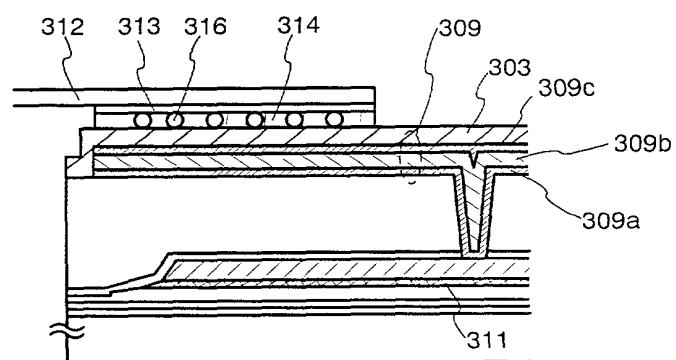


FIG. 10

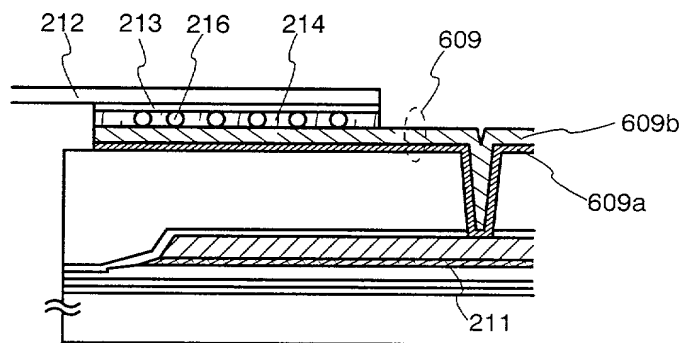


FIG. 11

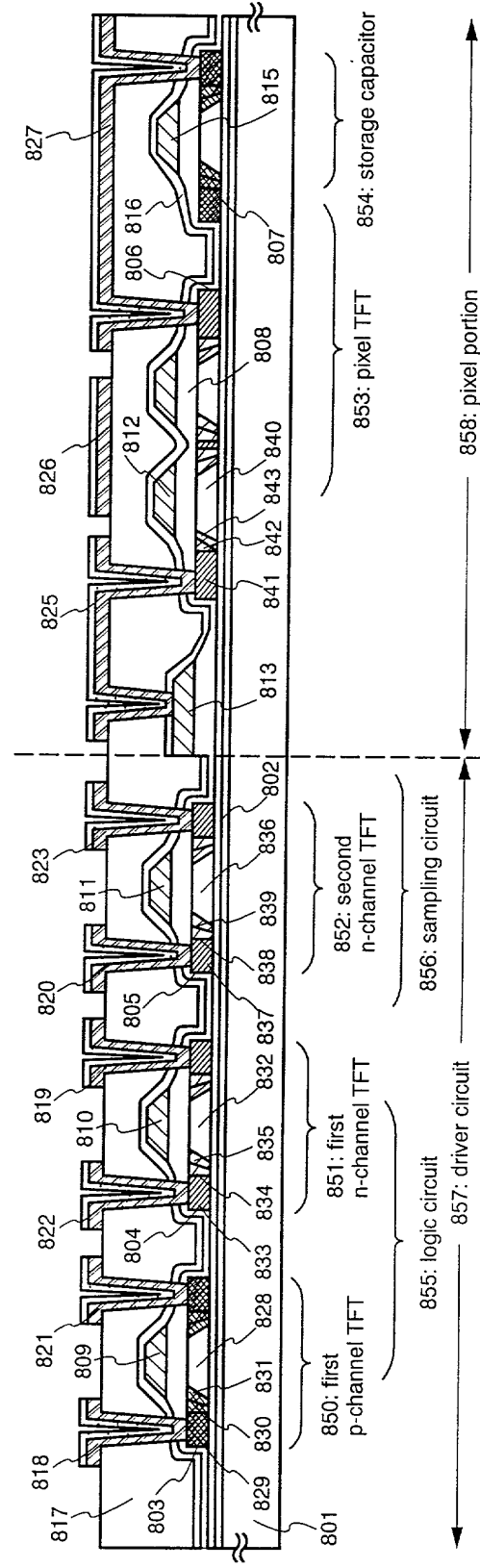


FIG. 12

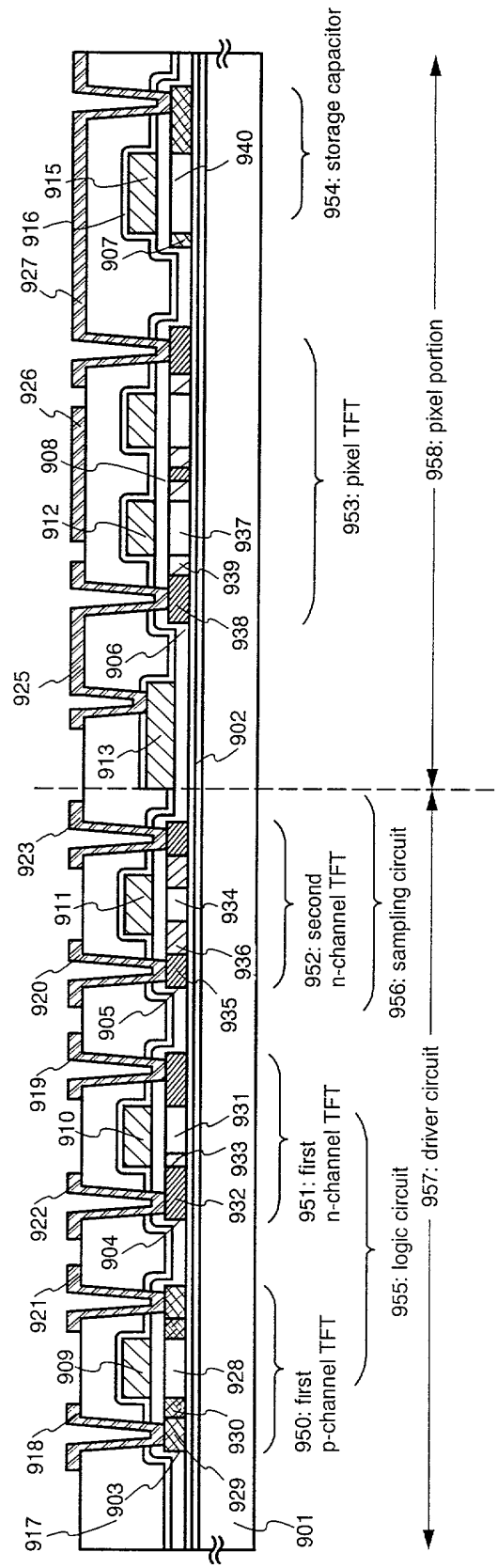




FIG. 14

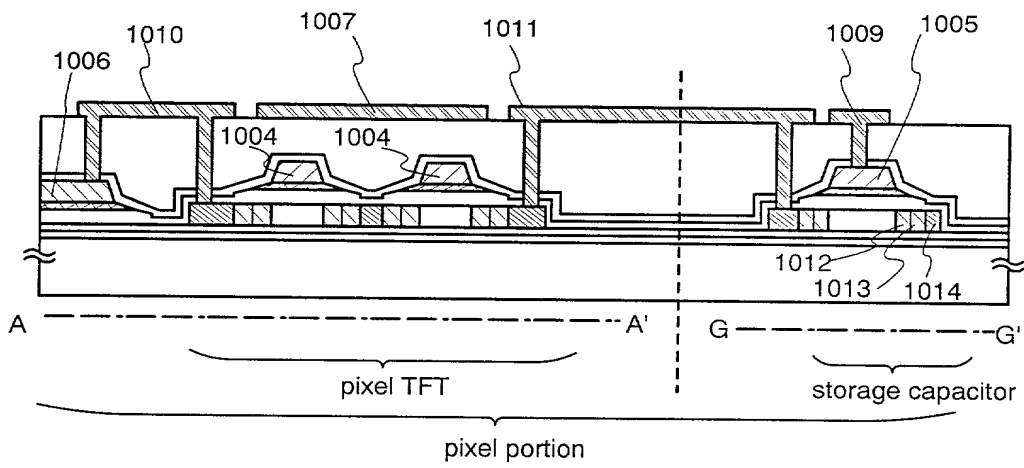


FIG. 15

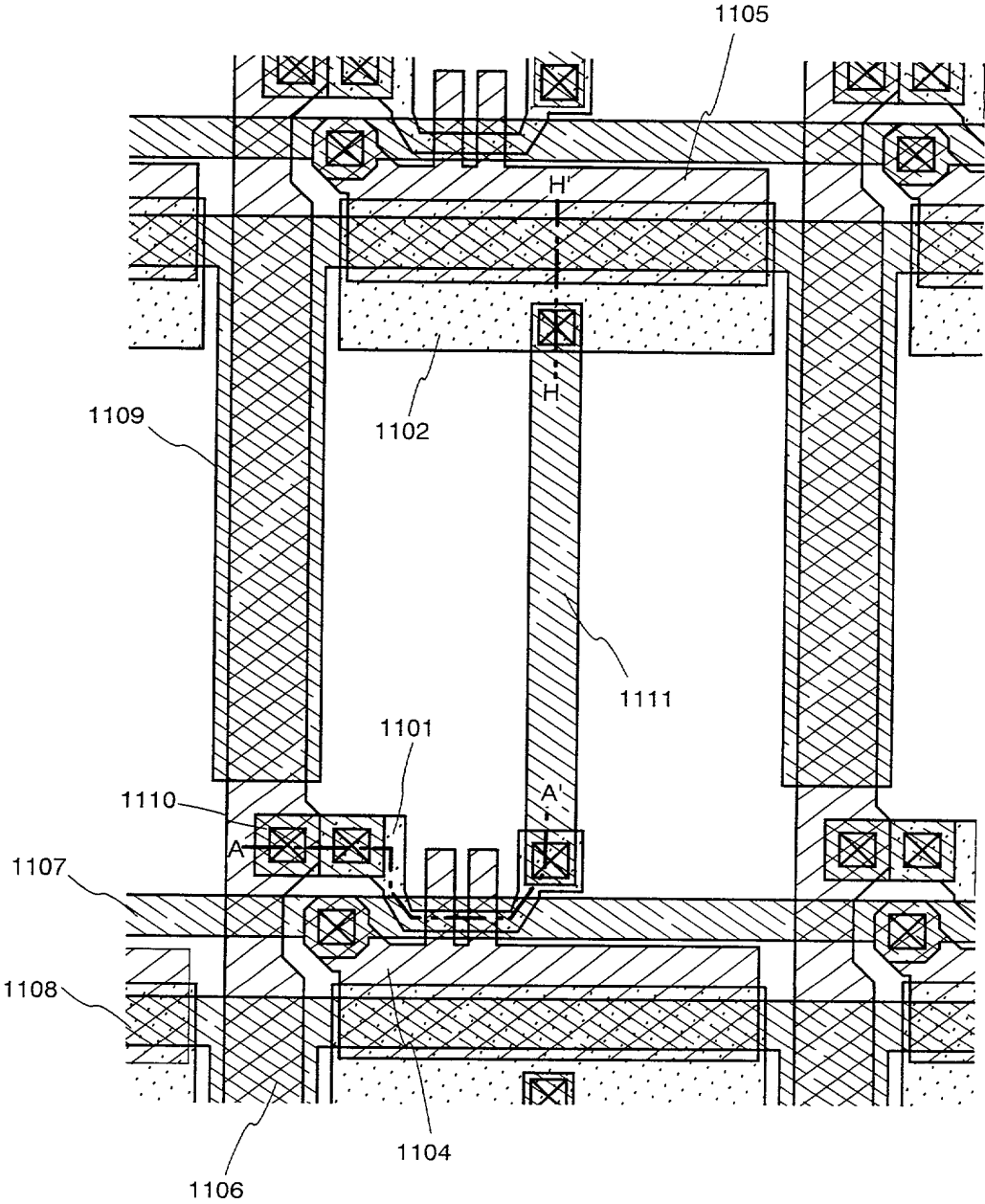


FIG. 16

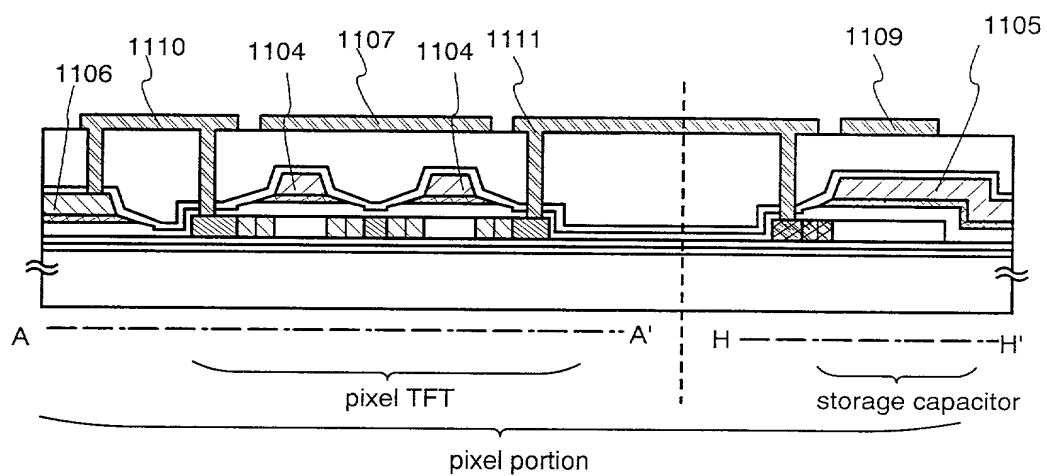




FIG. 17

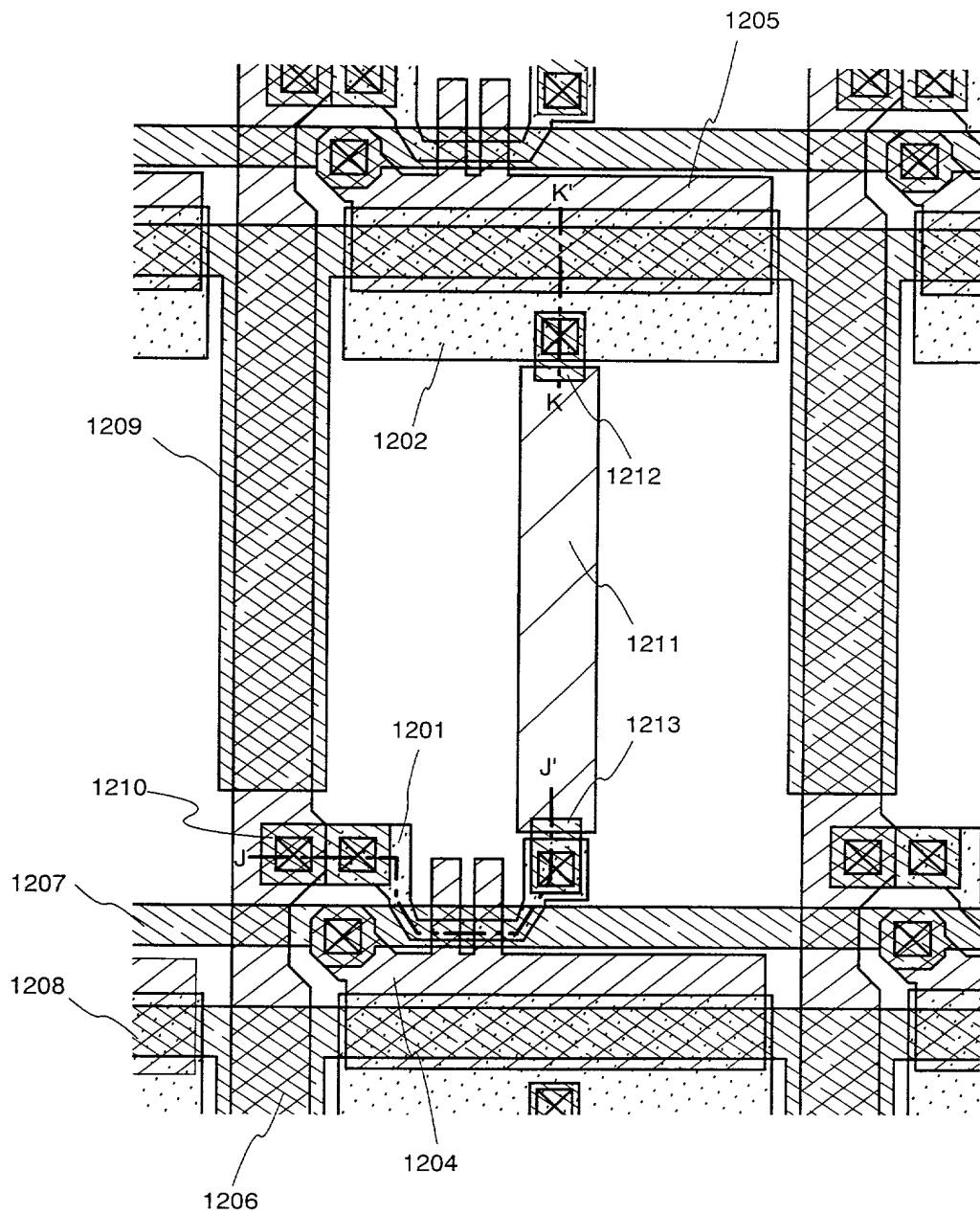


FIG. 18

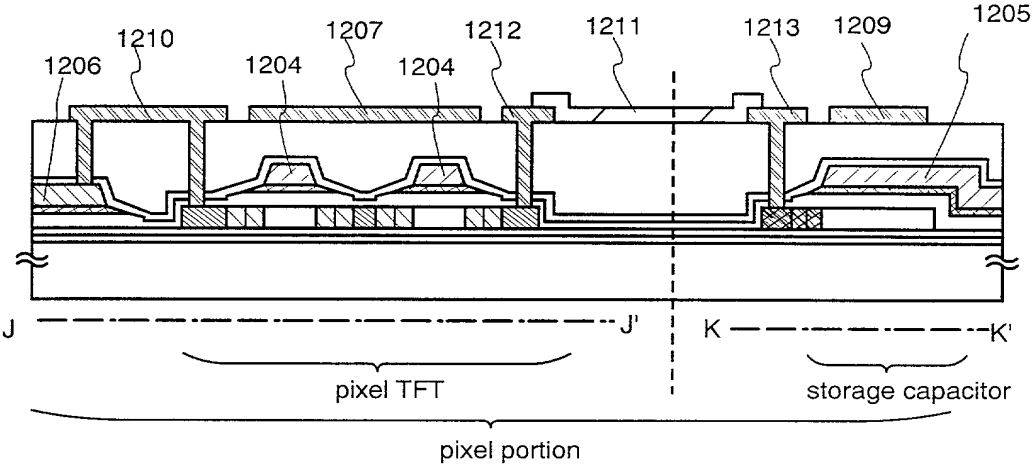
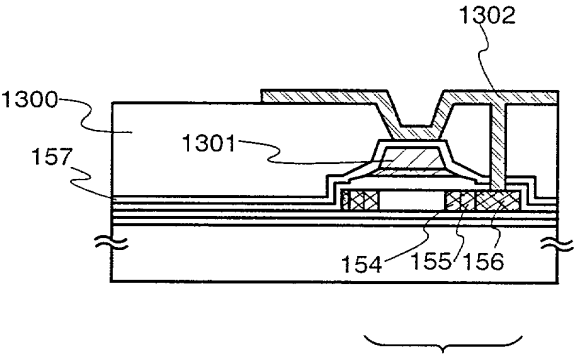


FIG. 19



405: storage capacitor

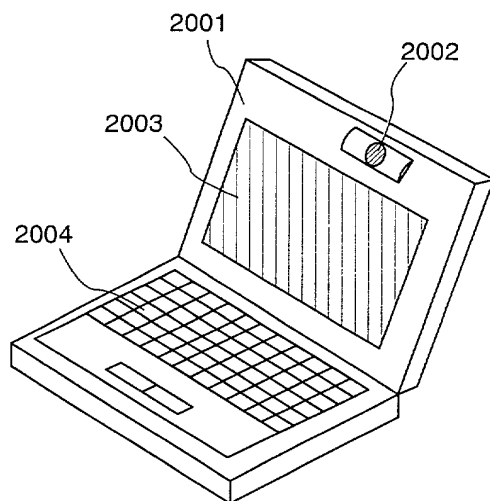


FIG. 20A

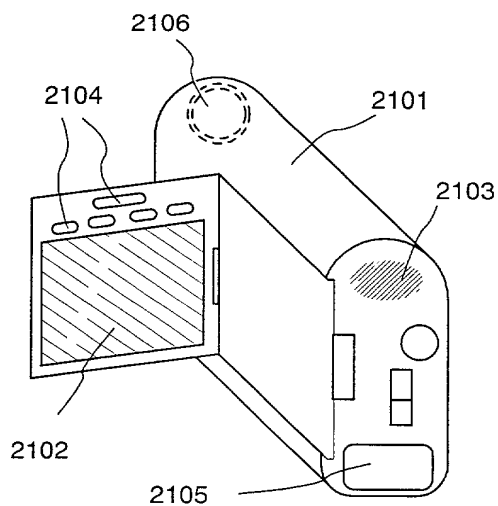


FIG. 20B

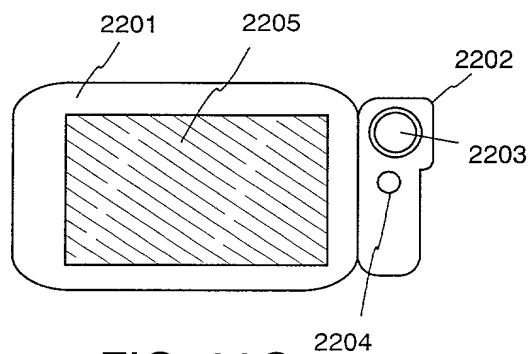


FIG. 20C

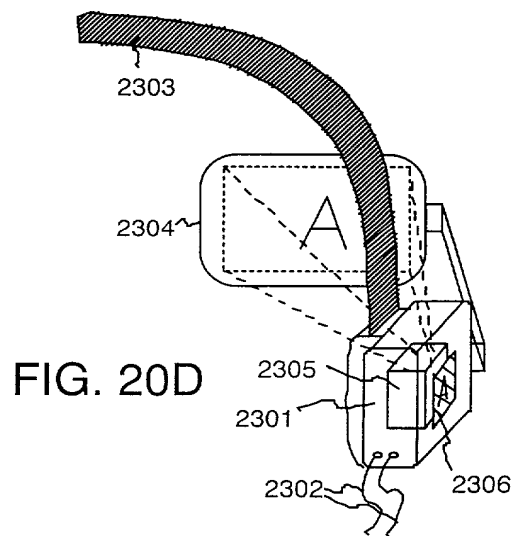


FIG. 20D

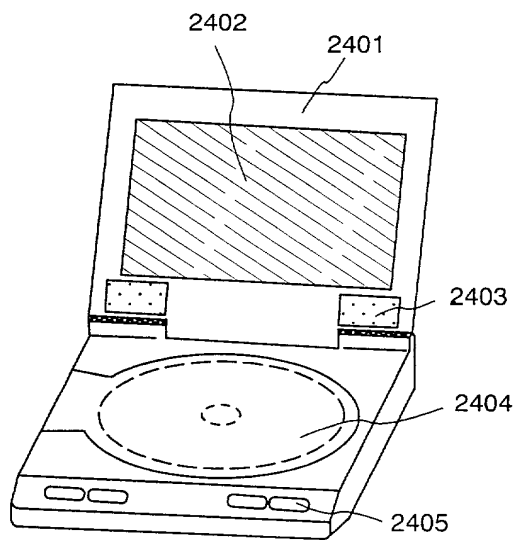


FIG. 20E

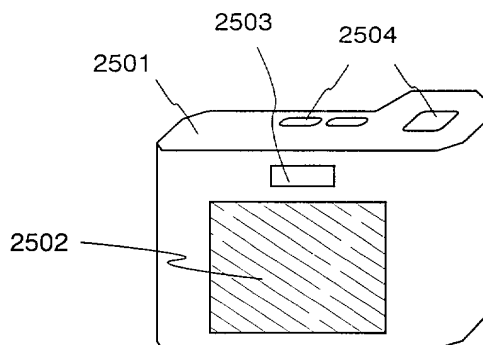


FIG. 20F

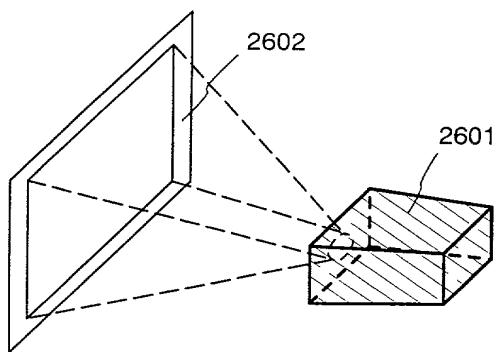


FIG. 21A

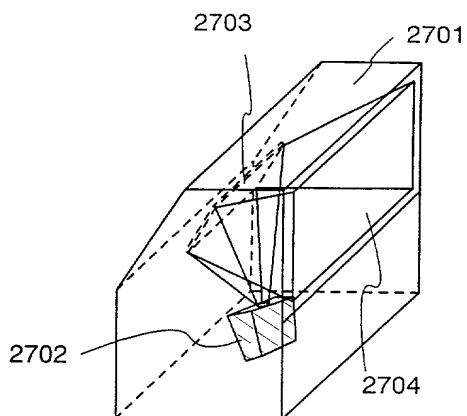


FIG. 21B

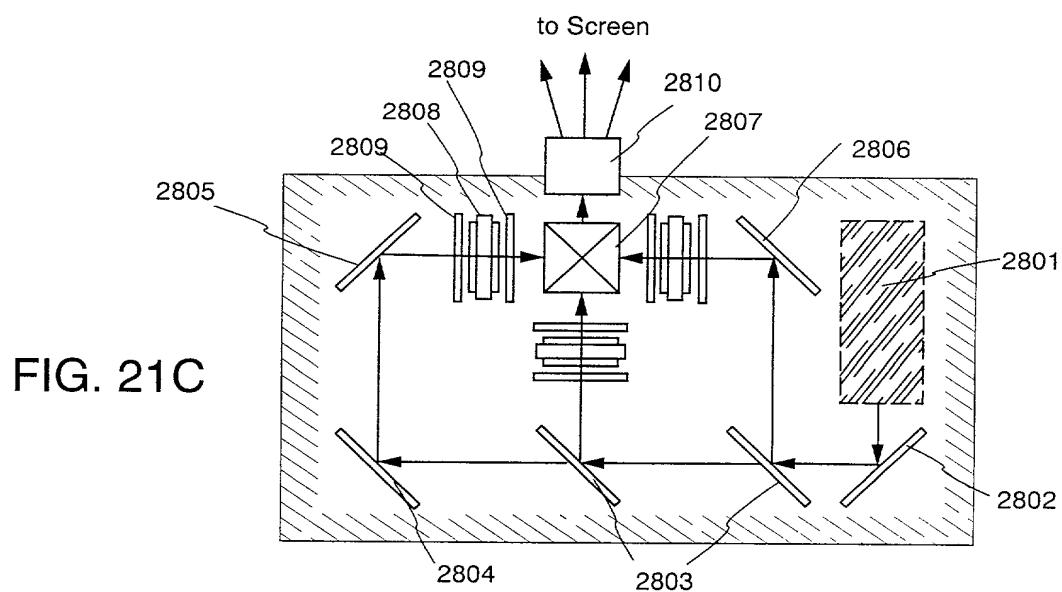


FIG. 21C

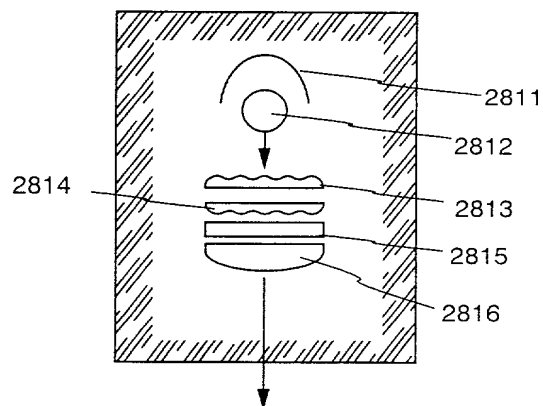


FIG. 21D

FIG. 22A

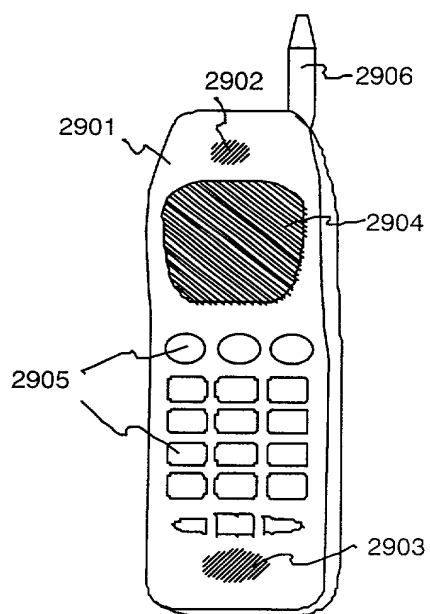


FIG. 22B

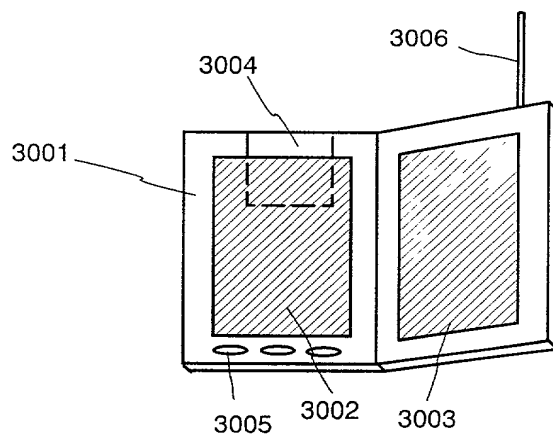


FIG. 22C

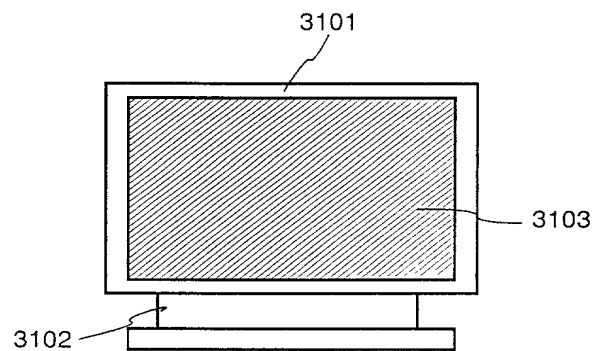


FIG. 23 prior art

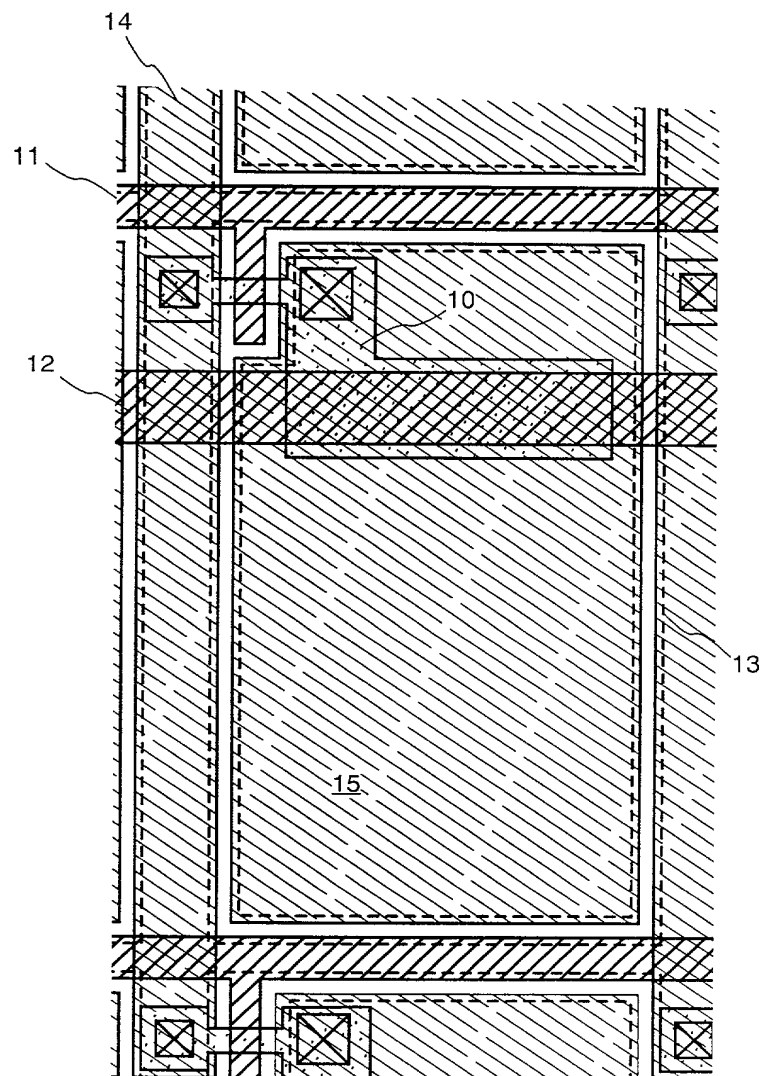


FIG. 24A

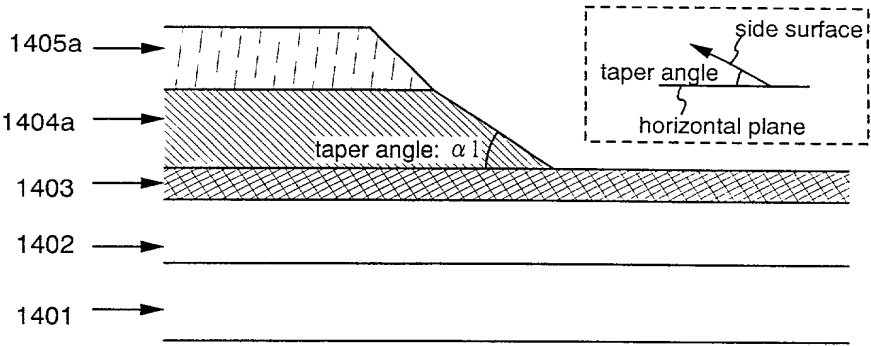


FIG. 24B

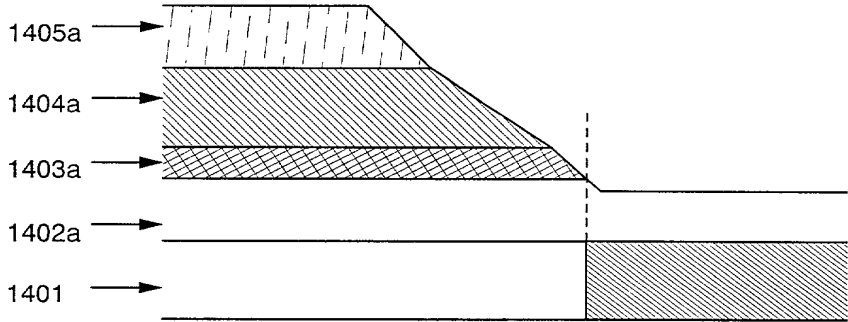


FIG. 24C

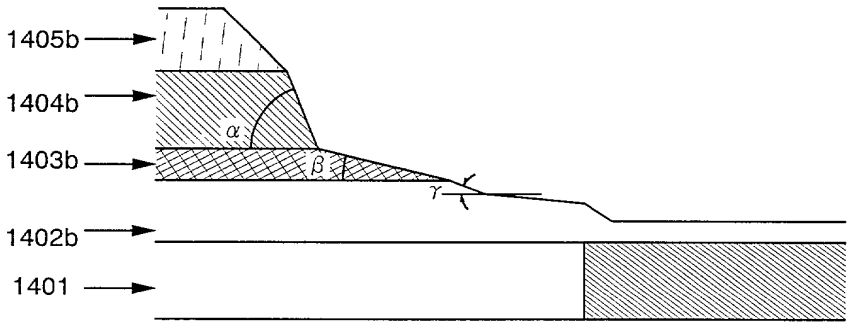


FIG. 24D

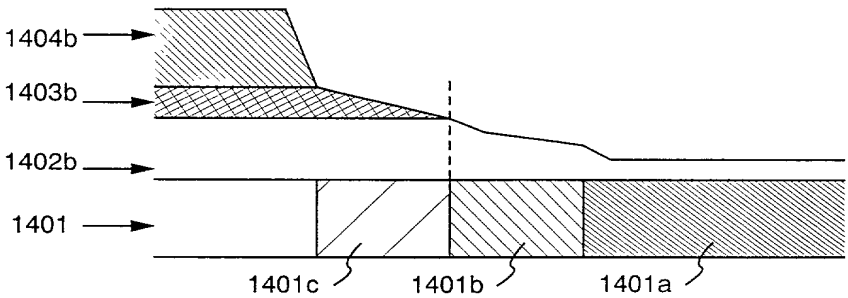




FIG. 25

